What is claimed is:

1. A method of forming a CMOS thin film transistor device on a substrate having an NMOS area, a PMOS area and a circuit area, the NMOS area having a first doped area, a lightly doped area and a first gate area, and the PMOS area having a second doped area and a second gate area, the method comprising the steps of:

(a) forming a semiconductor layer on the substrate;

(b) performing a first patterning process using a first photomask on the semiconductor layer to form a first semiconductor island and a second semiconductor island on part of the substrate, wherein the first semiconductor island is located in the NMOS area and the second semiconductor island is located in the PMOS area;

(c) forming a dielectric layer on the first semiconductor island, the second semiconductor island and the substrate;

(d) forming a metal layer on the dielectric layer;

(e) performing a second patterning process using a second photomask to form a first photoresist layer on the metal layer located in the lightly doped area, the first gate area, the PMOS area and the circuit area;

(f) using the first photoresist layer as a mask, removing part of the metal layer to form a first metal layer in the lightly doped area and the first gate area, a second metal layer in the PMOS area and a third metal layer in the circuit area, wherein the third

metal layer electrically connects the first metal layer and the second metal layer;

(g) using the first and the second metal layers as masks, performing an n^+-ion implantation to form a first source/drain region in the first semiconductor island in the first doped area;

(h) performing a dry etching procedure to remove part of the first photoresist layer, part of the first metal layer and part of the second metal layer, thus forming a first gate with a symmetrical cone shape, a remaining second metal layer and a remaining first photoresist layer, and exposing the dielectric layer in the lightly doped area, wherein a bottom width of the first gate is narrower than that of the first metal layer, and the symmetrically coned shape is gradually thinner from bottom to top;

(i) using the first gate and the remaining second metal layer as masks, performing an n^--ion implantation to form an LDD (lightly doped drain) region in the first semiconductor layer in the lightly doped area;

(j) removing the remaining first photoresist layer and thus forming an NMOS element in the NMOS area;

(k) performing a third patterning process using a third photomask to remove the remaining second metal layer in the second doped area, thus forming a second gate on the dielectric layer in the second gate area; and

(l) performing a p^+-ion implantation to form a second source/drain region in the second semiconductor island in the second doped area, thus forming a PMOS element in the PMOS area.

2. The method according to claim 1, wherein step (k) further comprises the steps of:

(k1) performing the third patterning process using the third photomask to form a second photoresist layer cover the NMOS area, the circuit area and the second gate area; and

(k2) using the second photoresist layer as a mask, removing the remaining second metal layer in the second doped area to form the second gate on the dielectric layer in the second gate area.

3. The method according to claim 2, wherein step (l) further comprises the step of:

(l1) using the second photoresist layer and the second gate as masks, performing the p^+-ion implantation to form the second source/drain region in the second semiconductor island in the second doped area and thus forming the PMOS element in the PMOS area.

4. The method according to claim 1, wherein the substrate is a glass substrate.

5. The method according to claim 1, wherein the first and the second semiconductor islands comprise silicon.

6. The method according to claim 1, wherein the dielectric layer is a SiO_x layer.

7. The method according to claim 1, wherein the metal layer comprises Mo.

8. The method according to claim 1, wherein part of the metal layer is removed by dry or wet etching.

9. The method according to claim 1, wherein an included angle at the bottom of the symmetrically coned shape is less than 45°.

10. The method according to claim 1, wherein an etching selectivity of the first photoresist layer to the metal layer ranges from 1 to 1/4.

11. A method of forming a CMOS thin film transistor device on a glass substrate having an NMOS area, a PMOS area and a circuit area, the NMOS area having a first doped area, a lightly doped area and a first gate area, and the PMOS area having a second doped area and a second gate area, the method comprising the steps of:

(a) forming a semiconductor layer on the substrate;

(b) performing a first patterning process using a first photomask on the semiconductor layer to form a first semiconductor island and a second semiconductor island on part of the glass substrate, wherein the first semiconductor island is located in the NMOS area and the second semiconductor island is located in the PMOS area;

(c) forming a silicon oxide (SiO_x) layer on the first semiconductor island, the second semiconductor island and the glass substrate;

(d) forming a molybdenum (Mo) layer on the silicon oxide layer;

(e) performing a second patterning process using a second photomask to form a first photoresist layer on the Mo layer located in the lightly doped area, the first gate area, the PMOS area and the circuit area;

(f) using the first photoresist layer as a mask, removing part of the Mo layer to form a first Mo layer in the lightly doped area and the first gate area, a second Mo layer in the PMOS area and a third Mo layer in the circuit area, wherein the third Mo layer electrically connects the first Mo layer and the second Mo layer;

(g) using the first and the second Mo layers as masks, performing an n^+-ion implantation to form a first source/drain region in the first semiconductor island in the first doped area;

(h) performing a dry etching procedure to remove part of the first photoresist layer, part of the first Mo layer and part of the second Mo layer, thus forming a first gate with a symmetrical cone shape, a remaining second Mo layer and a remaining first photoresist layer, and exposing the silicon oxide layer in the lightly doped area, wherein a bottom width of the first gate is narrower than that of the first metal layer, and the symmetrically coned shape is gradually thinner from bottom to top;

(i) using the first gate and the remaining second Mo layer as masks, performing an n^--ions implantation to form an LDD (lightly doped drain) region in the first semiconductor layer in the lightly doped area;

(j) removing the remaining first photoresist layer and thus forming an NMOS element in the NMOS area;

(k) performing a third patterning process using a third photomask to remove the remaining second Mo layer in the second doped area to form a second gate on the silicon oxide layer in the second gate area; and

(l) performing a p^+-ion implantation to form a second source/drain region in the second semiconductor island in the second doped area, thus forming a PMOS element in the PMOS area.

12. The method according to claim 11, wherein step (k) further comprises the steps of:

(k1) performing the third patterning process using the third photomask to form a second photoresist layer cover the NMOS area, the circuit area and the second gate area; and

(k2) using the second photoresist layer as a mask, removing the remaining second Mo layer in the second doped area to form the second gate on the silicon oxide layer in the second gate area.

13. The method according to claim 12, wherein step (l) further comprises the step of:

(l1) using the second photoresist layer and the second gate as masks, performing the p^+-ion implantation to form the second source/drain region in the second semiconductor island in the second doped area and thus forming the PMOS element in the PMOS area.

14. The method according to claim 11, wherein the first and the second semiconductor islands are polysilicon layers.

15. The method according to claim 11, wherein part of the metal layer is removed by dry or wet etching.

16. The method according to claim 11, wherein an included angle at the bottom of the symmetrical cone shape is less than 45°.

17. The method according to claim 11, wherein an etching selectivity of the first photoresist layer to the metal layer ranges from 1 to 1/4.

18. A method of forming a CMOS thin film transistor device on a substrate having at least one NMOS area, the NMOS area having a doped area, a lightly doped area and a gate area, the method comprising the steps of:

(a) forming a semiconductor layer on the substrate;

(b) patterning the semiconductor layer to form a semiconductor island in the NMOS area;

(c) forming a dielectric layer on the semiconductor island and the substrate;

(d) forming a metal layer on the dielectric layer;

(e) removing part of the metal layer to form a first metal layer in the lightly doped area and the gate area;

(f) using the first metal layer as a mask, performing an n^+-ion implantation to form a source/drain region in the semiconductor island in the doped area;

(g) performing a dry etching procedure to remove part of the first metal layer, thus forming a gate with a

symmetrical cone shape and exposing the dielectric layer in the lightly doped area, wherein a bottom width of the gate is narrower than that of the metal layer, and the symmetrical cone shape is gradually thinner from bottom to top; and

(h) using the gate as a mask, performing an n^--ion implantation to form an LDD (lightly doped drain) region in the semiconductor layer in the lightly doped area, and thus forming an NMOS element in the NMOS area.

19. The method according to claim 18, wherein an included angle at the bottom of the symmetrically coned shape is less than 45°.

20. The method according to claim 19, wherein an etching selectivity of the first photoresist layer to the metal layer ranges from 1 to 1/4.